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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,621	12/15/2003	Mitsuru Arai	OKI 399	8975

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,621	ARAI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of specie A (Figures 1-1 and 1-2) in the reply filed on 5/13/05 is acknowledged. Note that applicant indicated that claims 1-6 read on the elected specie A (Figures 1-1 and 1-2).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 contains so many indefinite problems so the metes and bounds of this claim is not clear. For example, in light of the specification, "one to a plurality of capacitors" on line 3 is indefinite because it is not clear whether applicant means "one" or "a plurality"; "one to a plurality of inverter circuitries" on line 6 is indefinite because it is not clear whether applicant means "one" or "a plurality"; "one to a plurality of switches" on line 7 3 is indefinite because it is not clear whether if applicant means "one" of "a plurality"; "one to a plurality of gated inverters" on lines 12-13 is indefinite because it is not clear whether if applicant means "one" of "a plurality". Further, "the capacitor of the initial stage" on lines 4 and 5 is indefinite due to the recitation "one to a plurality of capacitors" on line 3 is indefinite as discussed above so it is not clear if "the capacitor" is referred to which one of the capacitors if it was "a plurality of capacitors" (on line 3), and "the initial stage" lacks antecedent basis. Also, "respective stages" is

also indefinite since it is not clear whether the "respective stages" includes the initial stage or are additional stages of the initial stage, because it the respective stages are additional to the initial stage then it would be misdescriptive since it is seen in Figures 1-1 and 1-2 that the circuit includes only two stages so it is not clear which elements would be for the initial stage.

Claims 2-6 are indefinite because they include the indefiniteness of claim 1.

Also in claim 2, "a subsequent stage" is indefinite because it is not clear whether it is one of the respective stages, or additional to the respective stage.

Also in claim 3, "a plurality of control power supply lines" (line 3), "connected to any of the control power supply lines" (line 21) and "connected to any of the plurality of the control power supply lines" (line 23) cause the claim to be indefinite since it is inconsistent with what already claimed since independent claim 1 already clearly recited that each of the first and second logic circuit transistors of the plurality of the gated inverters connected to a first power supply line and a second power supply line, respectively, so it is not clear how can they also connected to any of the control power supply lines. Also, "plurality of control power supply lines" in claim 3 also indefinite because it is not clear whether they include the first and second power supply lines (recited in claim 1), or they are additional of the power first and second supply lines (recited in claim 1).

Also in claim 3, "the first logic circuit transistor", "the second logic transistor", "the first current control transistor" and "the second current control transistor" are indefinite because it is not clear the recited transistors are for which one of the gate inverters.

Also in claim 3, "connected to a constituent disposed in a preceding stage" is indefinite because it is not understood what applicant means by "connected to a constituent" (throughout

the claim), and "a preceding stage" is also indefinite because it is not clear whether it is one of the respective stages, or additional to the respective stage, or whether "preceding stage" is the same as the initial stage. Similarly, "connected to a constituent disposed in a subsequent stage" is also indefinite for the similar reason.

Also in claim 3, "the gated inverters in within the same inverter circuitry are connected to the control power supply lines at voltage level differing from each other" is indefinite since it is inconsistent with what already claimed. Note that independent claim 1 already recited that each of the first and second logic circuit transistors of the plurality of the gated inverters connected to a first power supply line and a second power supply line, respectively, so each of the gated inverters are connected between the first and second power supply lines and thus each of the gated inverters must have the same voltage supply. Thus, it is not clear how can they also be able to connected to the control power supply lines having differing voltages as recited in claim 3.

Claims 4-6 are also indefinite because they include the indefiniteness of claim 3.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueno (JP 7-264018).

Insofar as understood in claims 1 and 2, Figure 1 of the Ueno reference discloses a chopper comparator which includes: a first input terminal (VI) for receiving an analog input voltage, a second input terminal (VR) for receiving a reference voltage; at least one capacitor (C1, C2); a first switch (SW1), a second switch (SWR), at least one inverter circuitry (M1-M2-M5-M6, or M3-M4-M8-M7), initial stage (C1, SW1A, M1-M2-M5-M6), subsequence stage (C2, SW2A, M3-M4-M8-M7), at least one switch (SW1A, SW2A) for connecting between input and output of the at least one inverter circuitry. Note that inverter circuit (M1-M2-M5-M6, or M3-M4-M8-M7) comprising at least one gated inverter (M1-M2-M5-M6, or M3-M4-M8-M7) each comprising a first logic circuit transistor (M1 or M3), a second logic circuit transistor (M2 or M4), a first current control circuit transistor (M5 or M7), a second current control circuit transistor (M6 or M8), a first power supply line (Vdd), and second power supply line (GND). Note Figure 1, as discussed shows two capacitors (C1, C2), two inverter circuitries (M1-M2-M5-M6, and M3-M4-M8-M7) , two switches (SW1A, SW2A).

Conclusion

6. Because the scope of claims 3-6 cannot be determined due to the above noted indefiniteness problems, no prior arts can be applied against these claims at this time. Note that this is not an indication of allowability.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 28, 2005

LONG NGUYEN
PRIMARY EXAMINER